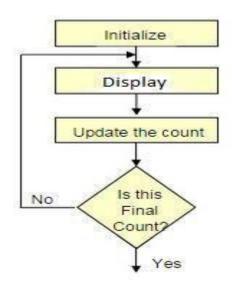
COUNTERS AND TIME DELAYS

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COUNTER AND TIME DELAYS

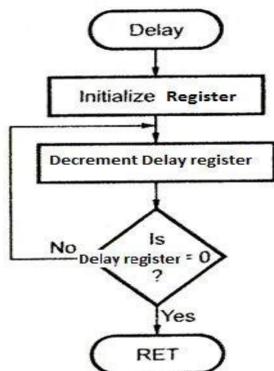
- A counter is designed simply by loading appropriate number into one of the registers and using INR or DNR instructions.
- Loop is established to update the count.
- Each count is checked to determine whether it has reached final number; if not, the loop is repeated.

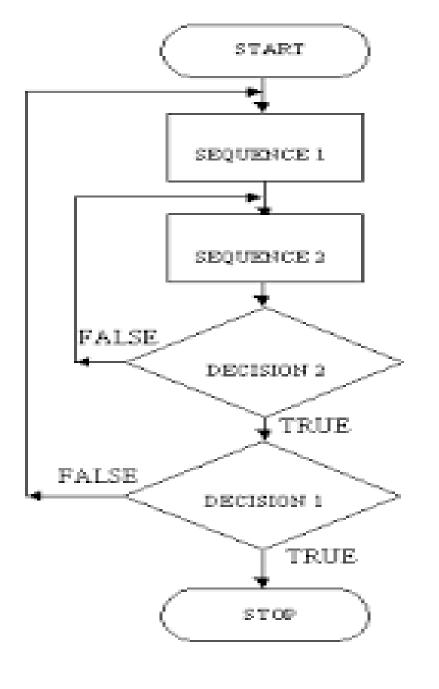


TIME DELAY

- Procedure used to design a specific delay.
- A register is loaded with a number, depending on the time delay required and then the register is decremented until it reaches zero by setting up a loop with conditional jump instruction.

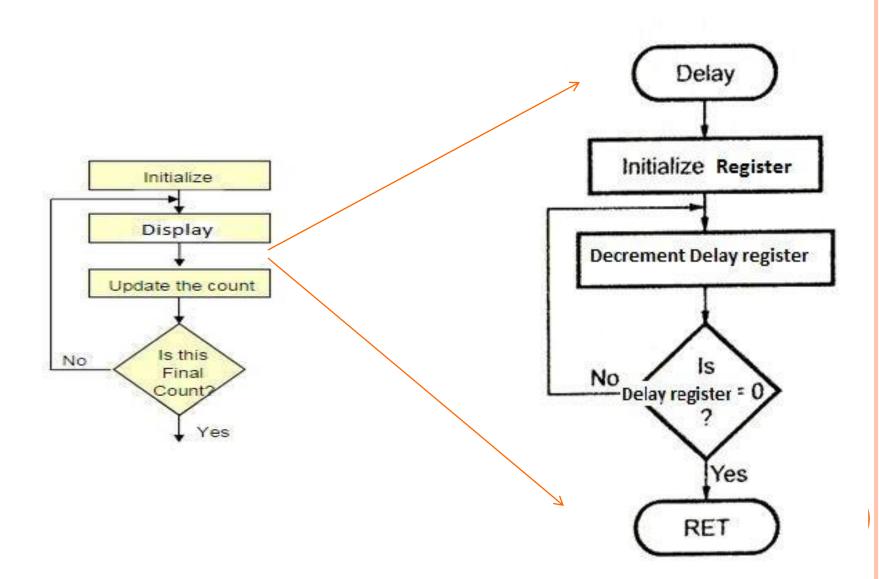
Time delay using One register:





Flowchart for tim e delay wit h two loops

Flowchart of a counter with time delay



ILLUSTRATIVE PROGRAM: HEXADECIMAL COUNTER

Write a Program to count continuously from FFH to ooH using register C with delay count 8oH between each count and display the number at one of the output ports.

MVI B,ooH

NEXT: DCR B

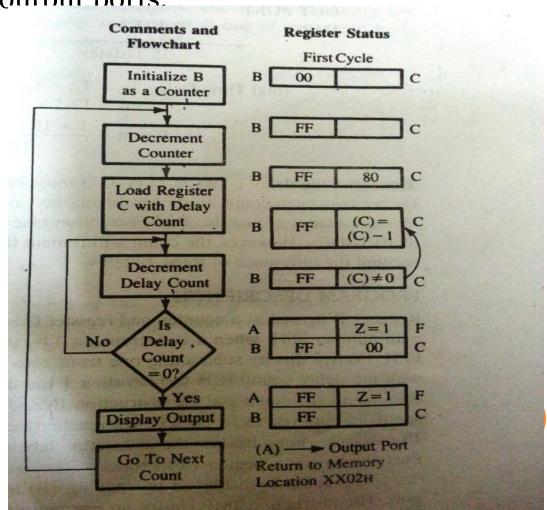
MVI C,80H

DELAY: DCR C

JNZ DELAY MOV A,B

OUT PORT#

JMP NEXT



ILLUSTRATIVE PROGRAM: ZERO TO NINE (MODULO TEN) COUNTER

START: MVI B,00H

MOVA,B

DSPLAY: OUT PORT#

LXI H,16-bit

LOOP:

DCX H

MOV A,L

ORA H

JNZ LOOP

INR B

MOV A,B

CPI 0AH

JNZ DSPLAY

JZ START

Start

Initialize counter Display

Output Load Delay

register

Decrement Delay register

Is Delay register=0?

Next Count 's count

=0AH?

If yes, Initialize counter If no, Display Output

ILLUSTRATIVE PROGRAM: GENERATING PULSE WAVEFORMS

MVI D, AAH X: MOV A, D

RLC

MOV D, A

ANI 01H

OUT PORT1

MVI B, COUNT

Y: DCR B JNZ Y JMP X •Generates a continuous square wave with the period of 500 Micro Sec. Assume the system clock period is 325ns, and use bit Do output the square wave.

•Delay outside loop: To=46 T states * 325=14.95 micro sec.

•Loop delay: TL=4.5 micro sec

•Total Td=To+TL Count=34 H



DEBUGGING COUNTER AND TIME DELAY PROGRAMS

- It is designed to count from 100(base 10) to 0 in Hex continuously with a 1 second delay between each count.
- The delay is set up using two loops. The inner loop is executed to provide approximately 100ms delay and is repeated 10 times, using outer loop to provide a total delay of 1 second.
- The clock period of system is 33ons.

MVI A, 64H	7
X: OUT PORT1	10
Y:MVI B, 10H	7
Z:LXI D, X	10
DCX D	6
NOP	4
NOP	4
MOV A, D	4
ORA E	4
JNZ Z	10/7
DCR B	4
JZ Y	10/7
DCR A	4
CPI 00H	7
JNZ X	10/7

Delay in loop1=32T X count x 330x10⁻⁹ 100ms =32T X count x 330x10⁻⁹ Count=9470